PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Ko et al.

Serial No.: 09/585,682

Filed: June 1, 2000

For: SEMICONDUCTOR DEVICE HAVING A SUBSTRATE, AN UNDOPED SILICON OXIDE STRUCTURE, AND AN OVERLYING DOPED SILICON OXIDE STRUCTURE WITH A SIDEWALL TERMINATING AT THE UNDOPED SILICON OXIDE STRUCTURE (Amended)

Confirmation No.: 7481

Examiner: C. Chu

Group Art Unit: 2815

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APPEAL BRIEF

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Attn: Board of Patent Appeals and Interferences

Sir:

This Appeal Brief is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

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I. REAL PARTY IN INTEREST

U.S. Application Serial No. 09/585,682 (hereinafter "the '682 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter "the Office") at Reel No. 9273, Frame No. 0990. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

II. RELATED APPEALS AND INTERFERENCES

The Board issued a decision in the appeal of the final rejection of U.S. Application Serial No. 09/625,144, which is related to the above-referenced application, on September 30, 2002. Appellants are not aware of any other related applications that are currently on appeal or subject to an interference proceeding before the Board that might influence the Board's decision in this Appeal.

III. STATUS OF CLAIMS

Claims 1-13 are currently pending and under consideration in the '682 Application.

Claims 1-13 stand rejected. The rejections of claims 1-13 are being appealed.

IV. STATUS OF AMENDMENTS

The '682 Application was filed on June 1, 2000, with thirteen (13) claims.

A first action on the merits of claims 1-13 was mailed on August 1, 2001. All of the claims were rejected under 35 U.S.C. §§ 101, 102, and 103. On October 30, 2001, an

Amendment responsive to the first action was mailed to the Office. Explanations as to the patentability of each of claims 1-13 were provided in that Amendment, and revisions to claims 6, 10, and 13 were presented.

A Final Office Action followed on February 15, 2002. In view of the explanations that had been provided by Appellants, the 35 U.S.C. §§ 101 and 103 rejections of claims 1-13 were withdrawn. The Examiner refused to withdraw the rejections under 35 U.S.C. § 102, however. On April 12, 2002, in a final attempt to convince the Examiner of the patentability of claims 1-13 over the cited art, a response to the Final Office Action was mailed.

An Advisory Action was then issued on May 3, 2002.

A Notice of Appeal dated May 13, 2002, promptly followed the Advisory Action, and was followed-up with an Appeal Brief, which was filed on July 15, 2002, which repeated the reasoning that had been presented in the response of April 12, 2002.

The Examiner, apparently having been convinced that the claim rejections that had been maintained were flawed, reopened prosecution by issuing another, non-final Office Action on November 20, 2002. Completely new grounds for rejecting claims 1-13 were presented in the Office Action of November 20, 2002. On February 20, 2003, Appellants submitted an Amendment that carefully explained the reasons that claims 1-13 are patentable over the then-new grounds of rejection. In that Amendment, claim 8 was revised.

Another non-final Office Action followed on May 30, 2003. Having again been convinced that the grounds for rejecting claims 1-13 that had been previously presented were not appropriate under the law, the Examiner presented new art in an attempt to show that claims 1-13

are not patentable. On August 29, 2003, another Amendment was mailed. In that Amendment, the new rejections were addressed, and claim 1 was amended.

This third set of rejections was maintained in a Final Office Action dated November 7, 2003. An Amendment Under 37 C.F.R. § 1.116 was filed, by mail on January 7, 2004, in response to the Final Office Action, and included revisions to each of claims 1-13, as well as reasoning as to the patentability of each of these claims. No additional claim revisions have since been presented.

The rejections were again maintained in an Advisory Action that was mailed on February 10, 2004.

A Request for Continued Examination was filed on February 13, 2003, along with instructions to enter the claim revisions that were proposed in the Amendment Under 37 C.F.R. § 1.116.

On May 5, 2004, another non-final Office Action was mailed. Once again, the Office presented new grounds for rejecting claims 1-13. As with all of the prior rejections, careful reasoning as to the patentability of claims 1-13 was presented in a response that was mailed on July 29, 2004.

As evidenced by the rejections presented in the Final Office Action of November 1, 2004, the Examiner again chose to ignore Appellants' reasoning as to the patentabilty of claims 1-13. Nonetheless, in one last attempt to convince the Examiner that claims 1-13 are patentable, Appellants filed a response to the Final Office Action. That response was mailed to the Office on January 3, 2005.

The Examiner maintained his grounds for rejecting claims 1-13 by way of an Advisory Action that was issued on January 28, 2005.

That Advisory Action was quickly followed by a Notice of Appeal on February 1, 2005, which is followed by this Appeal Brief, which is being submitted within two months of the date on which the Notice of Appeal was mailed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claims of the '682 Application are directed to semiconductor devices that include passivation structures with one or more sidewalls that are oriented substantially perpendicular to a plane of a substrate and that terminate at undoped silicon oxide structures.

In independent claim 1, the passivation structure is a passivation layer that covers one or more conductive lines. The sidewall is the sidewall of a contact aperture that extends through the passivation layer. It terminates at an undoped silicon dioxide cap over a conductive line.

The passivation structure of independent claim 6 is a doped silicon oxide structure.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-13 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in U.S. Patent 5,286,344 to Blalock et al. (hereinafter "Blalock"), in view of teachings from U.S. Patent 5,428,240 to Lur (hereinafter "Lur").

VII. ARGUMENT

Each of claims 1-13 is patentable under 35 U.S.C. § 103(a) for reciting subject matter which is not obvious over that taught in Blalock, in view of teachings from Lur.

A. APPLICABLE LAW

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

B. REFERENCES RELIED UPON

Blalock

Blalock teaches use of anisotropic etchants (col. 6, lines 31-52) that have selectivity for doped or undoped silicon dioxide over silicon nitride (*see* col. 6, lines 9-16) to form contact apertures through a passivation layer of a semiconductor device structure. Col. 6, lines 31-33; *see also* col. 4, line 4, to col. 5, line 41; col. 6, line 53, to col. 9, line 26. The resulting semiconductor device structure includes a semiconductor substrate, at least one conductive line disposed upon an active surface of the semiconductor substrate, sidewall spacers flanking the at least one conductive line, and a silicon nitride cap over the at least one conductive line. The

substantially perpendicular relative to the semiconductor substrate. At least a portion of the at least one sidewall terminates at an interface between the passivation layer and the undoped silicon dioxide cap.

Independent claim 6 is directed to a semiconductor device that includes a semiconductor substrate, at least one undoped silicon oxide structure, and at least one doped silicon oxide structure over the at least one undoped silicon oxide structure. The at least one doped silicon oxide structure includes at least one sidewall that is oriented substantially perpendicular to a plane of the semiconductor substrate. At least a portion of the at least one sidewall terminates at an interface between the at least one doped silicon dioxide structure and the at least one undoped silicon oxide structure.

While the claims clearly recite structures rather than processes, it should be noted that one of ordinary skill in the art would readily recognize that certain types of processes may not be used to form certain structural features. For example, it would be apparent to one of ordinary skill in the art that a contact aperture with a sidewall that is oriented substantially perpendicular to a semiconductor substrate (independent claim 1) or a plane of the substrate (independent claim 6) could not be formed by isotropic etch processes, which remove material in all directions at the same rate. *See, e.g.,* Wolf, Silicon Processing for the VLSI Era—Vol. 1, page 522 (Lattice Press, 1986) (hereinafter "Wolf"), a copy of the relevant pages of which have already been provided. Consequently, the processes that are used to form prior art structures may be relevant to the applicability of such references to the claims that are currently pending in the above-referenced application.

passivation layer, which is located over the silicon nitride cap, includes the contact apertures, which have sidewalls that are oriented substantially perpendicular to the semiconductor substrate and that terminate at the silicon nitride cap.

Lur

Lur teaches semiconductor device structures that include etch stop layers that may also function as caps for conductive lines. The etch stop layers are preferably formed from silicon nitride, but may also be formed from boron nitride or undoped silicon dioxide. Col. 5, lines 29-35. While Lur notes that the etch stop layers taught therein have a greater etching resistance than that of an overlying borophosphosilicate glass (BPSG) layer (col. 5, lines 32-35), Lur provides no indication as to whether an undoped silicon dioxide etch stop layer would be effective or useful when an anisotropic etch process is used to remove material of the BPSG layer to form a sidewall from the BPSG layer that is oriented substantially perpendicular to a substrate over which the BPSG and etch stop layers are formed.

C. ANALYSIS

Independent claim 1 recites a semiconductor device that includes a semiconductor substrate, at least one conductive line on an active surface of the semiconductor substrate, sidewall spacers flanking the at least one conductive line, and an undoped silicon dioxide cap over and in contact with the at least one conductive line. In addition, a passivation layer is disposed over the undoped silicon dioxide cap. At least one contact aperture is defined through the passivation layer. The at least one contact aperture includes at least one sidewall that extends

It is respectfully submitted that a *prima facie* case of obviousness has not been established against independent claim 1, independent claim 6, or any of claims 2-5 or 7-13 depending therefrom for at least two reasons.

No Motivation to Combine the Reference Teachings

First, before the priority date for the above-referenced application, one of ordinary skill in the art would not have been motivated to combine the teachings of Blalock and Lur in such a way as to render the subject matter in any of these claims obvious.

More specifically, it is respectfully submitted that neither Blalock nor Lur provides any teaching or suggestion that would motivate one of ordinary skill in the art to effect a process thtat would result in the semiconductor device structures that are recited in claims 1-13 of the above-referenced application. While the teachings of Blalock are directed to silicon oxide etching processes in which silicon nitride is useful as an etch stop, but that do not discriminate between doped silicon oxides and undoped silicon oxides (*see* col. 6, lines 9-16), Lur fails to explain whether or not anisotropic etch processes may be used etch a BPSG (doped silicon dioxide) layer when undoped silicon dioxide is used to form an etch stop layer 28 (col. 5, lines 29-35). *See also* Wolf, page 529, which suggests that wet etch processes may be anisotropic, and page 539, which suggests that dry etch processes may be isotropic.

Thus, neither Blalock nor Lur provides a clear teaching or suggestion that the etch process disclosed therein could be used to form a side wall having the characteristics required by independent claims 1 and 6 of the above-referenced application (*i.e.,* a sidewall that extends substantially perpendicular relative to a substrate (independent claim 1) or a plane of the

substrate (independent claim 6) and that at least a portion of the sidewall terminates at an interface between the passivation layer (independent claim 1) or doped silicon oxide structure (independent claim 6) by which the sidewall is defined and an undoped silicon oxide structure).

Accordingly, it is respectfully submitted that Blalock and Lur would not have provided one of ordinary skill in the art with any motivation to combine the teachings of these references in such a way as to replace the silicon nitride caps of Blalock with an undoped silicon oxide etch stop, as taught in Lur. Rather, the only source for such motivation appears to have been hindsight provided by the disclosure of the above-referenced application.

No Reasonable Expectation of Success

Second, it is respectfully submitted that one of ordinary skill in the art would have had no reason to expect that the asserted combination of teachings from Blalock and Lur would have resulted in the structures recited in claims 1-13 of the above-referenced application. If the undoped silicon oxide etch stop were merely substituted for the silicon nitride layer of Blalock, due to lack of selectivity for the disclosed etchant between doped and undoped silicon oxides, etching of the overlying doped silicon dioxide layer would continue on into the undoped silicon dioxide film. Lur also fails to teach or suggest any specific etchants that could be used to form sidewalls having the characteristics that are recited in independent claims 1 and 6. Therefore, one of ordinary skill in the art would have no reason to expect the asserted combination of teachings from Blalock and Lur to be successful.

In view of the foregoing, it is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 1-13. Thus, each of claims 1-13

recites subject matter which is allowable over the teachings of Blalock and Lur. It is, therefore, requested that the 35 U.S.C. § 103(a) rejections of claims 1-13 be reversed.

VIII. CLAIMS APPENDIX

The current status of each claim that has been introduced into the above-referenced application is set forth in CLAIMS APPENDIX to this Appeal Brief.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132. Accordingly, no evidence appendix accompanies this Appeal Brief.

X. RELATED PROCEEDINGS APPENDIX

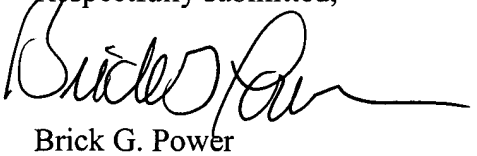
No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a related proceedings appendix.

XI. CONCLUSION

It is respectfully submitted that each of claims 1-13 is patentable under 35 U.S.C. § 103(a) for reciting subject matter which is not obvious over that taught in Blalock, in view of teachings from Lur.

Accordingly, the rejections of claims 1-13 should be reversed, and each of these claims should be allowed.

Respectfully submitted,



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CLAIMS APPENDIX

1. A semiconductor device, comprising:

a semiconductor substrate including an active surface;

at least one conductive line disposed upon the active surface, the at least one conductive line being flanked by sidewall spacers;

an undoped silicon dioxide cap disposed over and in contact with the at least one conductive line;

a passivation layer over the undoped silicon dioxide cap; and

at least one contact aperture defined through the passivation layer and including at least one sidewall extending substantially perpendicularly relative to the semiconductor substrate, at least a portion of the at least one sidewall terminating at an interface between the passivation layer and the undoped silicon dioxide cap.

2. The semiconductor device of claim 1, wherein the at least one conductive line comprises a word line.

3. The semiconductor device of claim 1, wherein the passivation layer comprises doped silicon dioxide.

4. The semiconductor device of claim 1, wherein the passivation layer comprises borophosphosilicate glass, phosphosilicate glass, or borosilicate glass.

5. The semiconductor device of claim 1, wherein the undoped silicon dioxide cap is at least partially exposed through the at least one contact aperture.

6. A semiconductor device, comprising:

a semiconductor substrate;

at least one undoped silicon oxide structure; and

at least one doped silicon oxide structure over the at least one undoped silicon oxide structure and having at least one sidewall substantially perpendicular to a plane of the semiconductor substrate, at least a portion of the at least one sidewall terminating at an interface between the at least one doped silicon dioxide structure and the at least one undoped silicon oxide structure.

7. The semiconductor device of claim 6, wherein the at least one sidewall comprises a sidewall of an aperture.

8. The semiconductor device of claim 6, wherein the at least one sidewall at least partially defines an aperture through the at least one doped silicon oxide structure.

9. The semiconductor device of claim 6, wherein the at least one doped silicon oxide structure comprises borophosphosilicate glass, phosphosilicate glass, or borosilicate glass.

10. The semiconductor device of claim 6, wherein the at least one undoped silicon oxide structure is at least partially located over a conductive structure.

11. The semiconductor device of claim 10, wherein the at least one undoped silicon oxide structure comprises an insulative cap over a conductive line.

12. The semiconductor device of claim 11, wherein the insulative cap is partially exposed through an aperture of the at least one doped silicon oxide structure defined by the at least one sidewall.

13. The semiconductor device of claim 6, wherein the at least one undoped silicon oxide structure is at least partially exposed adjacent the at least one sidewall.